

WHAT IS CLAIMED IS:

1 1. A computer instruction comprises:
2 a move and duplicate instruction that causes a processor
3 to load a first portion of bits of a source into a first
4 portion of a destination register and duplicate that first
5 portion of bits in a subsequent portion of the destination
6 register.

1 2. The instruction of claim 1 in which the first portion of
2 the source is 64-bits representing a double floating point
3 data type in a memory location.

1 3. The instruction of claim 1 in which the first portion of
2 the source is 64-bits representing a double floating point
3 data type in a source register.

1 4. The instruction of claim 1 in which the first portion of
2 the destination register is loaded with bits [63-0] of the
3 first portion of the source and the subsequent portion of the
4 destination register is loaded with bits [63-0] of the first
5 portion of the source.

1 5. A method comprising:
2 in a processor, loading a first portion of bits of a
3 source into a first portion of a destination register; and

4 duplicating the first portion of bits in a subsequent
5 portion of the destination register.

1 6. The method of claim 5 in which the first portion of the
2 source is 64-bits representing a double floating point data
3 type in a memory location.

1 7. The method of claim 5 in which the first portion of the
2 source is 64-bits representing a double floating point data
3 type in a source register.

1 8. The method of claim 5 in which the first portion of the
2 destination register is loaded with bits [63-0] of the first
3 portion of the source and the subsequent portion of the
4 destination register is loaded with bits [63-0] of the first
5 portion of the source.

1 9. A computer program product residing on a computer
2 readable medium having instructions stored thereon which, when
3 executed by the processor, cause the processor to:

4 load a first portion of bits of a source into a first
5 portion of a destination register; and
6 duplicate the first portion of bits in a subsequent
7 portion of the destination register.

1 10. The computer program product of claim 9 in which the
2 first portion of the source is 64-bits representing a double
3 floating point data type in a memory location.

1 11. The computer program product of claim 9 in which the
2 first portion of the source is 64-bits representing a double
3 floating point data type in a source register.

1 12. The computer program product of claim 9 in which the
2 first portion of the destination register is loaded with bits
3 [63-0] of the first portion of the source and the subsequent
4 portion of the destination register is loaded with bits [63-0]
5 of the first portion of the source.

1 13 A computer instruction comprises:
2 a move one double floating point and duplicate
3 instruction that causes a processor to load 64-bits of a
4 source and return the 64-bits in a lower half of a destination
5 and a upper half of a destination.

1 14. The instruction of claim 13 further comprising:
2 a source operand; and
3 a destination operand.

1 15. The instruction of claim 13 in which the source operand
2 is a memory location.

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1 16. The instruction of claim 15 in which the memory location
2 has a 128-bit value that represents a double floating point
3 data type.

1 17. The instruction of claim 13 in which the source operand
2 is a 128-bit source register.

1 18. The instruction of claim 17 in which the source register
2 has a 128-bit value that represents a double floating point
3 data type.

1 19. A method executed in a processor comprising:
2 loading a first number N of bits from a source into a
3 lower half of a $2N$ wide-bit destination register and in a
4 upper half of the $2N$ -bit wide destination register.

1 20. The method of claim 19 in which the source is a memory
2 location and where N is 64 bits.

1 21. The method of claim 20 in which the memory location
2 contains a double floating point data type.

1 22. The method of claim 19 in which the source is a 128-bit
2 source register and N is 64 bits.

1 23. The method of claim 19 in which the 128-bit source
2 register contains a double floating point data type.

1 24. A computer program product residing on a computer
2 readable medium having instructions stored thereon which, when
3 executed by the processor, cause the processor to:

4 load 64-bits from a source in a lower half of a 128-bit
5 destination register and in an upper half of the 128-bit
6 destination register.

1 25. The computer program product of claim 24 in which the
2 source is a memory location containing a 128-bit double
3 floating point data type.

1 26. The computer program product of claim 24 in which the
2 source is a 128-bit source register containing a 128-bit
3 double floating point data type.

1 27. A computer instruction comprises:

2 a move packed single floating point high and duplicate
3 instruction that causes a processor to load bits [127-0] of a
4 source and return bits [63-32] of the source in bits [31-0] of
5 a 128-bit destination register, bits [63-32] of the source in
6 bits [63-32] of the destination register, bits [127-96] of the
7 source in bits [95-64] of the destination register and bits
8 [127-96] of the source in bits [127-96] of the destination
9 register.

1 28. The instruction of claim 27 further comprising:
2 a source operand field; and
3 the destination operand field.

1 29. The instruction of claim 27 in which the source operand
2 is a memory location.

1 30. The instruction of claim 29 in which the memory location
2 has 128-bits representing a packed single floating point data
3 type.

1 31. The instruction of claim 27 in which the source operand
2 is a 128-bit source register.

1 32. The instruction of claim 31 in which the source register
2 has 128-bits representing a packed single floating point data
3 type.

1 33. A method executed in a processor comprising:
2 accessing bits [127-0] of a source; and
3 returning bits [63-32] of the source in bits [31-0] and
4 bits [63-32] of the destination register; and
5 bits [127-96] of the source in bits [95-64] and bits
6 [127-96] of the destination register.

1 34. The method of claim 33 in which the source is a memory
2 location.

1 35. The method of claim 34 in which the memory location
2 contains a packed single floating point data type.

1 36. The method of claim 33 in which the source is a 128-bit
2 source register.

1 37. The method of claim 36 in which the 128-bit source
2 register contains a packed single floating point data type.

1 38. A computer program product residing on a computer
2 readable medium having instructions stored thereon which, when
3 executed by the processor, cause the processor to:

4 load bits [127-0] of a source;

5 return bits [63-32] of the source in bits [31-0] of a
6 128-bit destination register;

7 return bits [63-32] of the source in bits [63-32] of the
8 destination register;

9 return bits [127-96] of the source in bits [95-64] of the
10 destination register; and

11 return bits [127-96] of the source in bits [127-96] of
12 the destination register.

1 39. The computer program product of claim 38 in which the
2 source is a memory location.

1 40. The computer program product of claim 39 in which the
2 memory location contains a packed single floating point data
3 type.

1 41. The computer program product of claim 38 in which the
2 source is a 128-bit source register.

1 42. The computer program product of claim 41 in which the
2 128-bit source register contains a packed single floating
3 point data type.

1 43. A computer instruction comprises:
2 a move a packed single floating point low and duplicate
3 instruction that causes a processor to load bits [127-0] of a
4 source and return bits [31-0] of the source in bits [31-0] of
5 a 128-bit destination register, bits [31-0] of the source in
6 bits [63-32] of the destination register, bits [95-64] of the
7 source in bits [95-64] of the destination register and bits
8 [95-64] of the source in bits [127-96] of the destination
9 register.

1 44. The instruction of claim 43 further comprising:
2 a source address field; and
3 the destination register.

1 45. The instruction of claim 44 in which the source is a
2 memory location.

1 46. The instruction of claim 45 in which the memory location
2 contains 128-bits representing a packed single floating point
3 data type.

1 47. The instruction of claim 43 in which the source is a 128-
2 bit source register.

1 48. The instruction of claim 47 in which the source register
2 contains 128-bits representing a packed single floating point
3 data type.

1 49. A method comprising:
2 in a processor, loading bits [127-0] of a source;
3 returning bits [31-0] of the source in bits [31-0] of a
4 128-bit destination register;
5 returning bits [31-0] of the source in bits [63-32] of
6 the destination register;
7 returning bits [95-64] of the source in bits [95-64] of
8 the destination register; and
9 returning bits [95-64] of the source in bits [127-96] of
10 the destination register.

1 50. The method of claim 49 in which the source is a memory
2 location.

1 51. The method of claim 50 in which the memory location
2 contains a packed single floating point data type.

1 52. The method of claim 51 in which the source is a 128-bit
2 source register.

1 53. The method of claim 52 in which the 128-bit source
2 register contains a packed single floating point data type.

1 54. A computer program product residing on a computer
2 readable medium having instructions stored thereon which, when
3 executed by the processor, cause the processor to:

4 load bits [127-0] of a source;

5 return bits [31-0] of the source in bits [31-0] of a 128-
6 bit destination register;

7 return bits [31-0] of the source in bits [63-32] of the
8 destination register;

9 return bits [95-64] of the source in bits [95-64] of the
10 destination register; and

11 return bits [95-64] of the source in bits [127-96] of the
12 destination register.

1 55. The computer program product of claim 54 in which the
2 source is a memory location.

1 56. The computer program product of claim 55 in which the
2 memory location contains a packed single floating point data
3 type.

1 57. The computer program product of claim 54 in which the
2 source is a 128-bit source register.

1 58. The computer program product of claim 57 in which the
2 128-bit source register contains a packed single floating
3 point data type.

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